REMARKS

Reconsideration and allowance of the present application are respectfully requested. Claims 1-3, 11-13, and 15-20, and 23-35 are currently pending in this application.

Record of January 23, 2006 Telephonic Interview

A telephonic interview was conducted on January 23, 2006 at the request of the undersigned. Participating in the interview were the undersigned and Examiner Joni Hsu. The undersigned thanks the Examiner for the courtesies extended during that interview.

In the interview, the undersigned presented an overview of the arguments to be set forth below in the current Response. The Examiner stated that the Patent Office would consider the Applicant's arguments upon presentation of a written response. No agreement was reached during the interview as to the allowability of the claims.

Regarding the 35 U.S.C. § 103 Rejections

Claims 1-3, 6, 9, 11-13, 16, 19, and 26-30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Published Application No. 20040054689A1 to Salmonsen et al. (referred to below as "Salmonsen") in view of U.S. Patent No. 6,611,269 to Uehara et al. (referred to below as "Uehara"). Applicant respectfully traverses this rejection for the following reasons.

Neither Salmonsen nor Herrera, whether considered alone or in combination, discloses the subject matter of the claims. For example, consider independent claim 1, reproduced below in its entirety:

1. A method for processing video data in an apparatus including a computer processing module and a graphics processing module, comprising:

receiving a principal video stream from a source via plural inputs to the graphics processing module, the plural inputs associated with respective components of the principal video stream;

receiving a video sub-stream containing supplemental information associated with the principal video stream via another input to the graphical processing module;

in a single stage operation, performing, by the graphics processing module, an operation on the principal video stream and combining the principal video stream with the video sub-stream to produce processed data, wherein the single stage operation requires only a single read transaction to perform the single stage operation; and

outputting the processed data,

wherein each of the plural inputs for receiving the principal video stream and the other input for receiving the video sub-stream refer to separate inputs, and

wherein the graphics processing module executes video processing tasks using a 3D graphics pipeline.

The primary reference, Salmonsen, describes an emulator interface that can analyze content communications to determine supported content formats, determine the format of presented content, and reformat or transcode the content to place the presented content in the supported format (note paragraph 0007 of Salmonsen). The video processing associated within this emulation can involve: removing an arbitrary frame region for processing; de-interlacing a video frame; enlarging or reducing video width or height; filtering for image resizing; removing an arbitrary frame region for encoding; downsampling of video width/height; video frame flipping or mirror imaging; gamma

correcting; anti-aliasing; and color manipulating (note, for example, the list enumerated in claim 18 of Salmonsen).

The secondary reference, Uehara, discloses a video processing unit 106 that includes a data selection means 1061 for reading out display data from an output buffer means 105. The data selection means 1061 selects data to be input to an arithmetic unit A 1062 and an arithmetic unit B 1063. Note column 8, lines 13-22 of Uehara. In one implementation, the arithmetic unit A 1062 performs the operation: α x A + β x B + C, and the arithmetic unit B 1063 performs the operation γ x D + (1- γ) x E, wherein A, B, C, D, and E represent video data selected by the data selection means 1061. That is, A is video data output from the output buffer means 105, B is video data which is the arithmetic operational result carried out in the past by the arithmetic units (1062, 1063), C is video data for background color or the like, D is video data of an on-screen display or the like, and E is video data selected by the data selection means 1061 from fixed value data (for example zero) or the like. See column 8, lines 34-61 of Uehara. Fig. 3 shows the operations performed by the arithmetic units (1062, 1063) according to one of Uehara's implementations. In these operations, the arithmetic units (1062, 1063) can perform, for instance, up-scaling and blending.

Neither Salmonsen nor Uehara disclose the invention recited in claim 1, whether these documents are considered alone or in combination. Representative deficiencies of these documents are outlined as follows.

First, claim 1 is directed to a method for processing video data in an "apparatus including a computer processing module and a graphics processing module." Claim 1 further recites that "the graphics processing module executes video processing tasks using a 3D graphics pipeline." Neither Salmonsen nor Uehara disclose a method that is performed in the context of the above-recited kind of environment. That is, Salmonsen's

emulator interface and Uehara's video processing unit 106 refer to functionality that is customized to meet specific video processing needs. This custom-tailored functionality cannot be characterized as a graphics processing module which executes video processing tasks using a 3D graphics pipeline in the manner recited in claim 1.

Second, claim 1 further recites "receiving a principal video stream from a source via plural inputs to the graphics processing module," "receiving a video sub-stream containing supplemental information associated with the principal video stream via another input to the graphical processing module, the plural inputs associated with respective components of the principal video stream," and "in a single stage operation, performing, by the graphics processing module, an operation on the principal video stream and combining the principal video stream with the video sub-stream to produce processed data." Claim 1 further recites that the "the single stage operation requires only a single read transaction to perform the single stage operation," and that "each of the plural inputs for receiving the principal video stream and the other input for receiving the video sub-stream refer to separate inputs." Neither Salmonsen nor Uehara, whether considered alone or in combination disclose this subject matter.

For instance, as discussed above, Salmonsen identifies a list of video processing operations including: removing an arbitrary frame region for processing; de-interlacing a video frame; enlarging or reducing video width or height; filtering for image resizing; removing an arbitrary frame region for encoding; downsampling of video width/height; video frame flipping or mirror imaging; gamma correcting; anti-aliasing; and color manipulating. Further, Salmonsen states that an emulator 800 can "generate a plurality of subpictures that overlay video for captions, sub-titles, karaoke, menus, and animation" (paragraph 0137). However, nowhere does Salmonsen disclose the type of "single stage" operation recited in claim 1. That is, there is absolutely no hint in Salmonsen that the

generating of subpictures (described in paragraph No. 0137) takes place in a single stage along with any other processing performed on a principal video stream.

In acknowledgement of the shortcomings of Salmonsen, the Office Action now relies on the Uehara document to address the "single stage" operation feature recited in claim 1. As discussed above, Uehara's two arithmetic units (1062, 1063) can perform upscaling and blending. And as identified in the passages cited in the Office Action, Uehara's two arithmetic units can operate in parallel fashion. However, the dual-unit functionality disclosed by Uehara does not comprise a graphics processing module for receiving a principal video stream and a video sub-stream on separate inputs in the manner recited in claim 1. For example, while figure 1 of Uehara shows multiple lines feeding into the two arithmetic units (1062, 1063), there is no hint that these lines comprise "plural inputs associated with respective components of the principal video stream."

Third, there is no motivation to combine Salmonsen and Uehara. Salmonsen is directed to emulator functionality to transcode video signals into a specified format. Uehara is directed to a video display unit 106, including a set top box for receiving digital broadcasting signals (column 1, lines 6 and 7 of Uehara). These two systems are tailored to suit specific objectives in the context of specific video processing environments. There is no indication that Salmonsen's system can benefit from Uehara's solutions, or vice versa, and thus, nothing links these documents together other than Patent Office's exercise of impermissible hindsight. The Office Action asserts that it would have been obvious to combine the teachings of these two documents to "speed processing." The Office Action further states that the "advances of parallel processing are well-known in the art." Note page 4, last paragraph, of the Office Action. However, these statements are generalities that ignore the concrete data processing environments disclosed by

Salmonsen and Uehara. Even if, assuming *arguendo*, that one of ordinary skill in the art wanted to apply parallel processing to Salmonsen in some fashion, Uehara's and Salmonsen's devices are so idiosyncratic and application-specific that there would have been no suggestion of how these devices could be combined. Moreover, the invention recited in claim 1 cannot be generalized as mere parallel processing when it recites a particular solution for single stage processing involving the receipt of specific inputs (as described above).

For at least the above-identified reasons, the Applicant submits that the combination of Salmonsen and Uehara does not render claim 1 obvious under 35 U.S.C. § 103. Independent claims 11 and 26-28 have been amended to recite related subject matter to claim 1, and are therefore allowable for reasons similar to those provided above.

The remaining claims that are rejected under Salmonsen and Uehara (i.e., claims 2, 3, 6, 9, 12, 13, 16, 19, 29, and 30) depend from the above-identified independent claims, and are allowable for at least this reason. These claims also recite additional features which are not disclosed in the either Salmonsen or Uehara, whether considered alone or combination.

Claims 5, 7, 8, 15, 17, 18, 21, 22, and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Salmonsen and Uehara, and further in view of U.S. Patent No. 6,208,350 to Herrara (referred to below as "Herrara"). Applicant respectfully traverses this rejection for the following reasons.

Claims 5, 7, 8, 17, and 18 depend variously from independent claim 1 or claim 11. Also, independent claim 25 has been amended to recite related subject matter to claim 1. These claims therefore distinguish over the base combination of Salmonsen and Uehara for reasons similar to those presented above. (Note that claims 21 and 22 have been canceled and therefore the rejection of these claims is rendered moot.)

Herrara does not remedy the deficiencies of Salmonsen and Uehara. More specifically, Herrara discloses the use of a graphics engine to perform motion compensation, YUV 4:2:0-to-4:2:2 conversion, and alpha blending. However, as pointed out in the previous Response, Herrara does not disclose (or suggest) the single stage processing recited in claim 1. Further, Herrara does not disclose the multi-input processing operations now recited in amended claim 1.

For the above reasons, the Applicant requests that the § 103 rejection based on Salmonsen, Uehara, and Herrara be withdrawn.

Claim 10 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Salmonsen and Uehara, and further in view of U.S. Patent No. 6,573,905 to MacInnis et al. (referred to below as "MacInnis"). Applicant respectfully traverses this rejection for the following reasons.

Claim 10 depends from independent claim 1, and is therefore allowable for at least this reason. MacInnis does not remedy the above-identified deficiencies of Salmonsen and Uehara, whether these documents are considered alone or in any combination. For instance, MacInnis does not disclose the single stage processing described above in the context of claim 1.

Moreover, McInnis does not disclose the claim elements for which it was cited. Namely, the Office Action added the McInnis document to address the recitation of a Uniform Memory Architecture (UMA) in claim 10. While UMA design, considered in a vacuum as a general concept, is not new, of course, MacInnis does not suggest the use of the above-described single stage processing in *conjunction* with UMA. The *combination* of the above-described single stage processing to UMA is particularly unique, as the single stage processing helps overcome some of the limitations of UMA in a non-obvious manner.

For the above reasons, the Applicant requests that the § 103 rejection based on Salmonsen, Uehara, and MacInnis be withdrawn.

Finally, claims 23 and 24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Salmonsen and Uehara, and further in view of U.S. Patent No. 6,753,878 to Heirich et al. (referred to as "Heirich"). Applicant respectfully traverses this rejection for the following reasons.

Claims 23 and 24 depend from independent claim 11, and are therefore allowable for at least this reason. Heirich does not remedy the above-identified deficiencies of Salmonsen and Uehara, whether these documents are considered alone or in any combination. For instance, Heirich does not disclose the single stage processing described above in the context of claim 1. Further, while Heirich discloses texture processing, there is no suggestion in Heirich of receiving the plural input streams as recited in claim 1. For example, Heirch does not disclose at least "receiving a principal video stream from a source via plural inputs to the graphics processing module, the plural inputs associated with respective components of the principal video stream," and "receiving a video sub-stream containing supplemental information associated with the principal video stream via another input to the graphical processing module."

Moreover, McInnis does not disclose the claim elements for which it was cited. Namely, there seems to be some confusion in the Office Action as to the purpose of the "texturing units" recited in claim 23. As amended, claim 23 recites, in part, that the "the graphics processing module includes multiple texturing units associated with the plural inputs and the other input." The Office Action states that texturing is well known:

> . . . .Texturing is a method of adding realism to a computer-generated graphic. A texture is added to a simpler shape, and this reduces the amount of computing needed to create shapes

> and textures in the scene. The trend has recently been towards larger and more varied texture images, together with increasingly sophisticated way to combine multiple textures for different aspects of the same object, and therefore texture is needed. Texturing is well-known in the art, widely used, and can be found many publications, such as the Wikipeidia Encyclopedia. (Page 16, second paragraph of the Office Action).

The Applicant does not dispute that texturing is well known in the environment that the Examiner mentions, namely the construction of three-dimensional scenes. However, the claimed subject matter uses texturing units in single stage processing in which a principal video stream is combined with a video sub-stream to produce processed data (as recited in claim 1). It is distinctly *not* known in the art to apply texturing in *this specific context*. It is well established in the case law that the application of a known technological component to a new use or in conjunction with a new combination of components may support patentable subject matter; this is the case here, as none of the applied documents discloses the application of different streams to different texturing units in the context of the subject matter recited in claims 1, 23, and 24.

For the above reasons, the Applicant requests that the § 103 rejection based on Salmonsen, Uehara, and Herich be withdrawn.

In conclusion, the Office Action generally attempts to establish a case for obviousness by considering each of the features recited in the claims in abstract isolation (such as parallel processing, UMA architecture, texturing, and so forth). But as clearly stated in MPEP § 2141.02, the claimed invention must be considered as a whole. Moreover, distilling the invention down to a "gist" or "thrust" (as by incorrectly interpreting the invention as an exercise of parallel processing or texturing, and so forth) disregards the requirement to consider the invention as a whole. The claims pass muster

under 35 U.S.C. § 103 and therefore the Applicant respectfully requests that all of the obviousness-type rejections be withdrawn.

Newly Added Claims

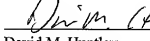
New claims 31-35 have been added in this Response. These claims depend variously on independent claims 1 and 25-28, and are allowable for at least this reason.

Conclusion

The arguments presented above are not exhaustive; Applicant reserves the right to present additional arguments to fortify its position. Further, Applicant reserves the right to challenge the alleged prior art status of one or more documents cited in the Office Action.

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and such allowance is respectfully solicited. The Examiner is urged to contact the undersigned if any issues remain unresolved by this Amendment.

Respectfully Submitted,

Dated: February 1, 2006 By: 

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